μPD65012C-132.

This custom LSI has to be used with 65030G-043 and 65040G-099.

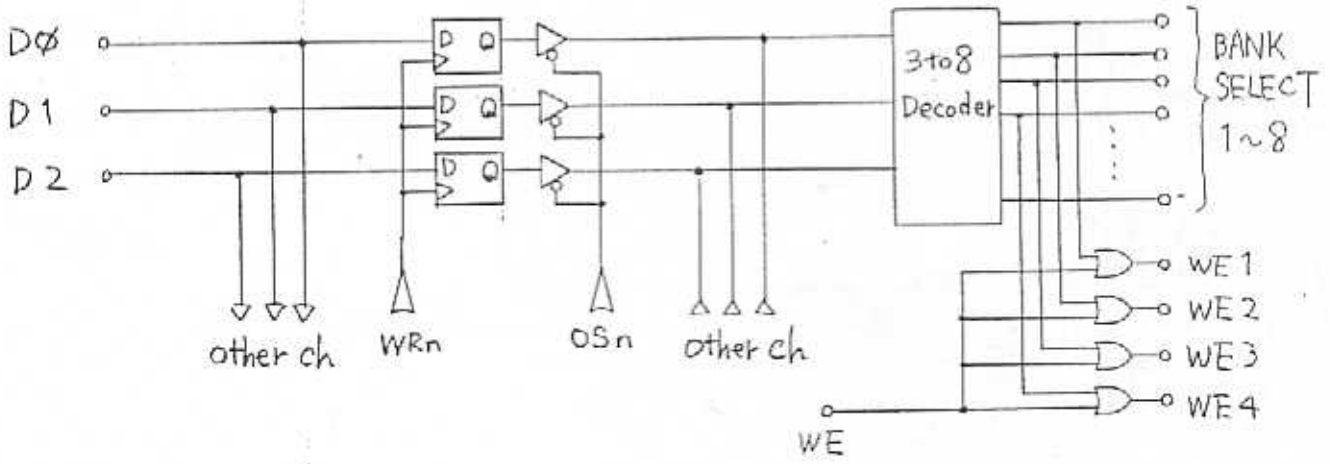
65040G-099 could only provide 18bit Address Data for 256k memory, But 65012c-132 can extend Address area 20bit:2Mword memory.

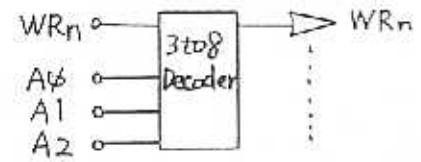
65012C-132 has 24ch×3bit Latch and 7 3to8 decoder(3 for Write pulse, 3 for output, 1 for Bank select).

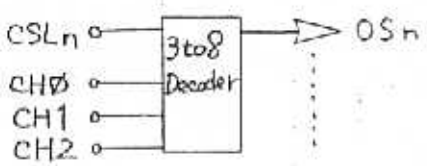
65012C-132 combined with 65030G-043 and 65040G-099, can extend Address area 8times DSS-1 but each sound must be in a certain BANK.

Bank select are for OE of 256k×4 type DRAM and synchronized with CSLn and CHn. WEn are provided for each BANK.

Now we are designing, it will be shown this NOV.







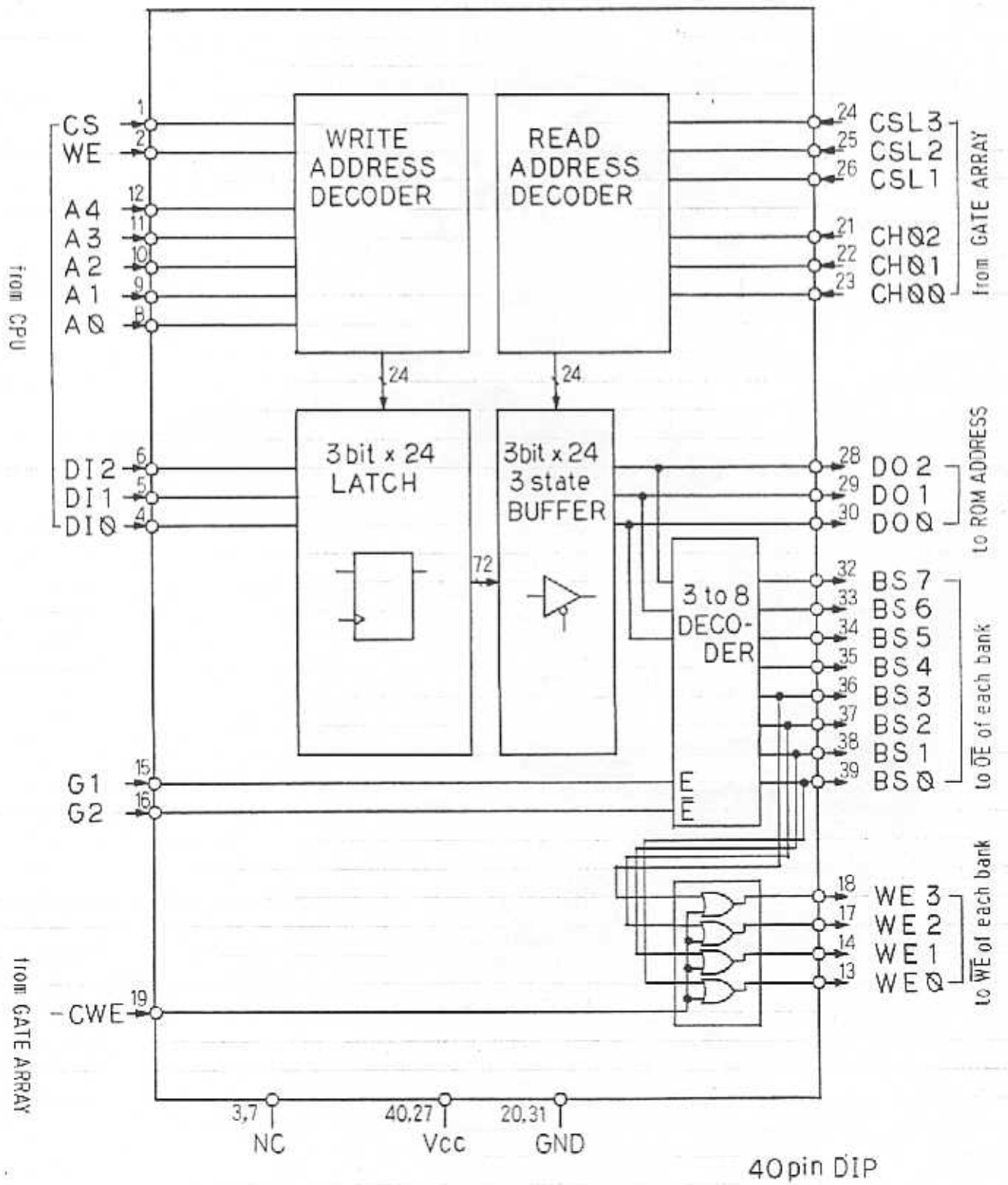
KORG

Subject: μPD65012C-132

No.

Date

Page



Approved	Checked	Made	Copy to
		吉野伸 61.10.22 技術部	

Total

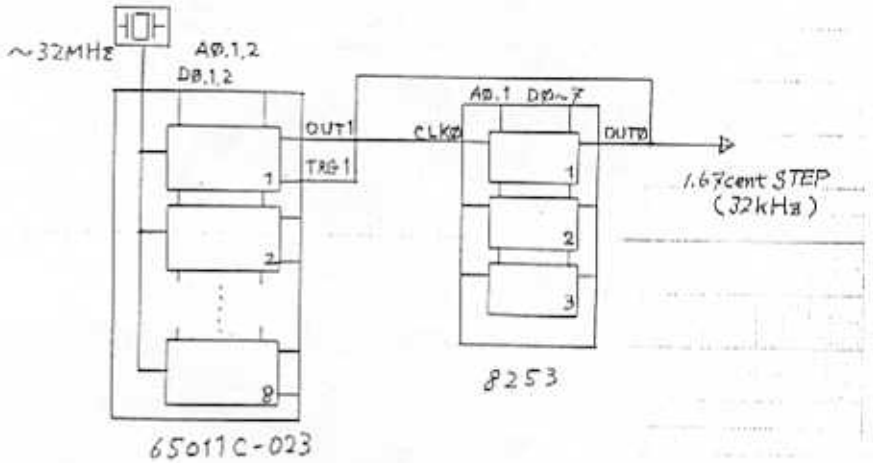
KF-50×200(S)

μPD65011C-023.

This custom LSI has to be used with 8253(16 bit programmable divider).

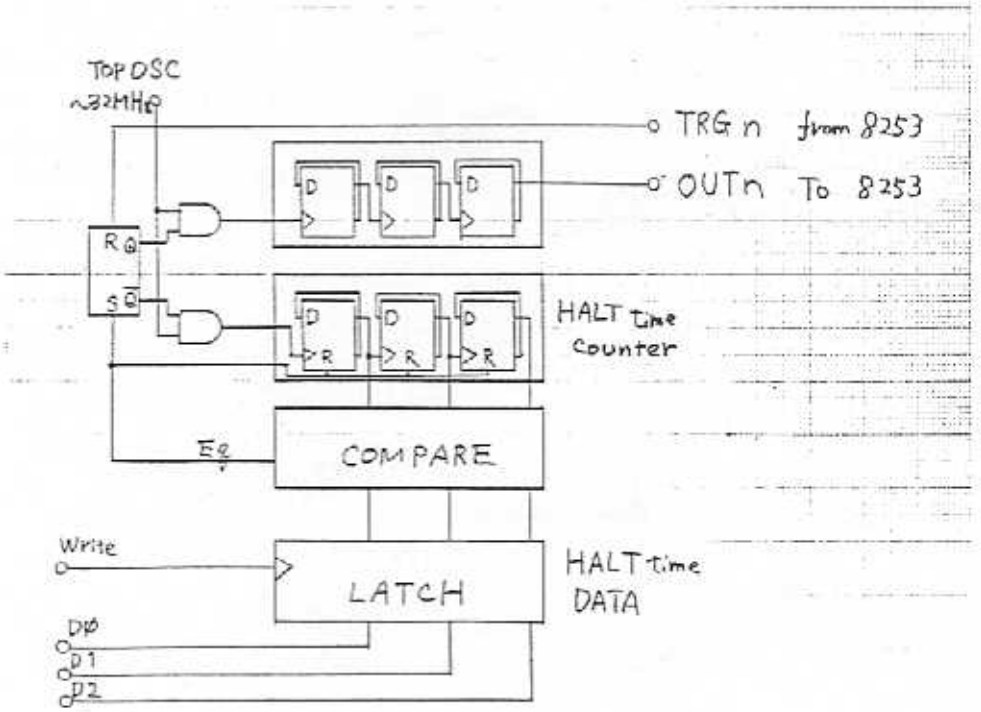
This LSI combined with 8253, works as 19bit divider and Top OSC can be up to 32MHz.

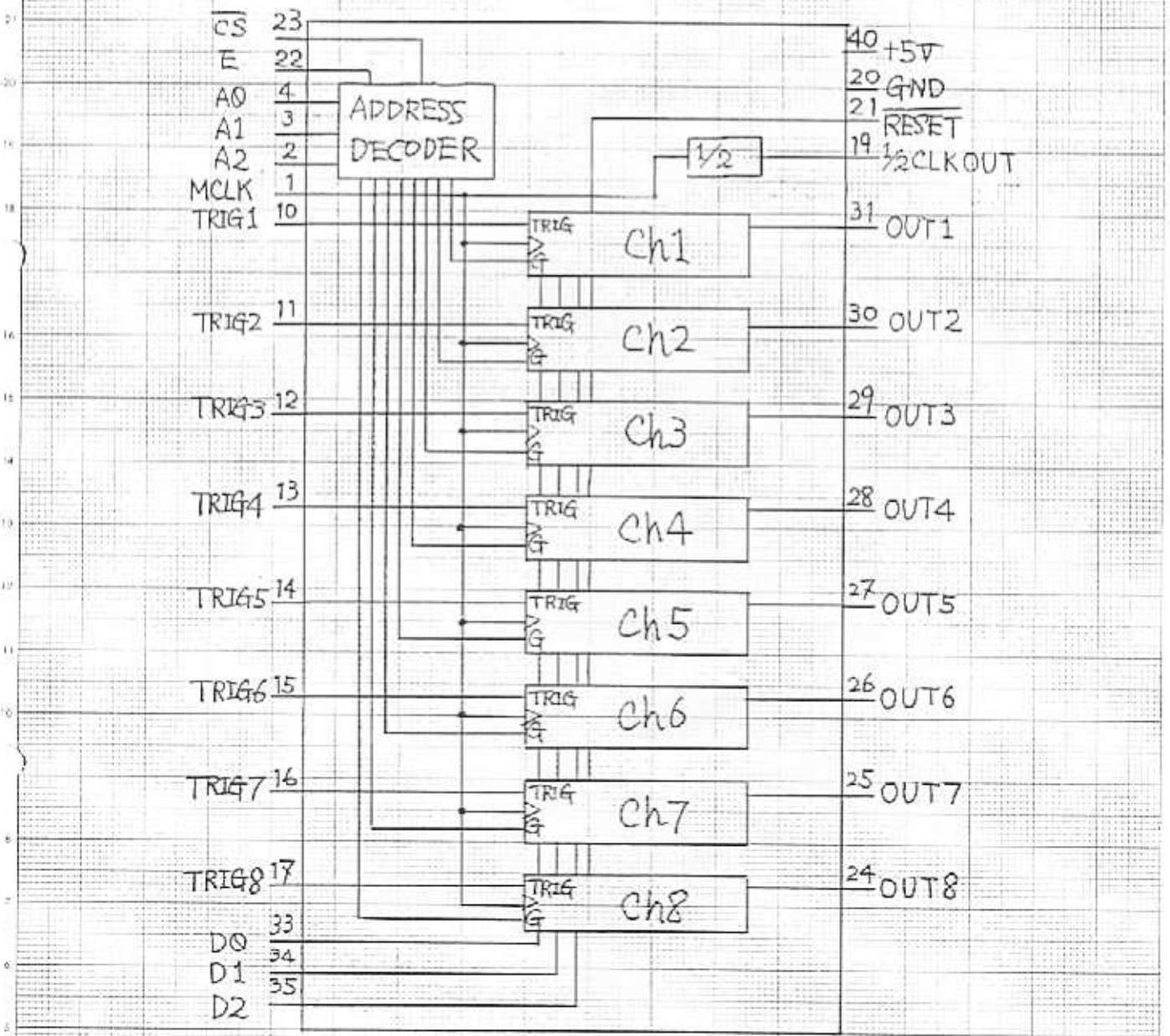
In this condition,minimum step of pitch is 1.67cent(32MHz sampling Freq.).



65011C-023 has 8blocks of 1/8 Divider with programmable HALT as following diagram.

BLOCK DIAGRAM (1 OSC)





μPD65011C-023

N.C. 5.6.7.8.9.18
32.36.37.38.39

μPD65030G-043 , μPD65040G-099.

In the DSS-1, since it is necessary to transfer a large quantity of data at high speed, the DMA (DIRECT MEMORY ACCESS) system is adopted. In this system, data are transferred directly between I/O and memory without going through the CPU registers. The LSIs developed for this purpose are the custom GATE ARRAY μPD65030G-043-12 (GA-I) and μPD65040G-099-12 (GA-II). The GA-I receives DMA requests on 16 channels (maximum of 24 channels), encodes them and generates timing. The GA-II stores 8 channels worth of memory addresses, increments addresses in response to requests and outputs in accordance with the GA-I timing.

In the DSS-1, two GA-IIs are needed for each GA-I to cover 16 channels.

< Caution > Both the GA-I and GA-II use 80-pin flat packages. Use caution in repair and replacement.

PROCEDURE OF DMA

To set new DMA address of key on channel.

0.Check MPUWE(MSB of 65030G-043).

1.Stop the DMA request clock from 8253 of key on channel.

2.Write the start address of wave memory to 65040G-099 data bus.(3 bytes)

3.Write end address of wave memory,loop sw and synchro sw to 65040G-099 data bus.(3 bytes)

4.write loop point address of wave memory to 65040G-099 data bus.When loop sw is off,it is not necessary.(3 bytes)

5.Write DMA ch to start ,read/write and zero cross start sw to 65030G-043 data bus.(1 byte)

6.Start DMA request clock.(sound pitch depends on it.)

Since 65040G-099 has 9bytes input buffer,Only one channel can be set New DMA address at one time.So before setting new DMA address ,it is necessary to check out finish to execute of DMA start already set.To check out this ,Read MSB of 65030G-043 data bus.

Loop sw,synch sw and zeroX start sw are not separated each DMA channel.Latest sw data written by MPU are effective all DMA channel.

Write pulse is provided only for ch0,other channel cannot be write mode.So during ch0 write,oter channel can read.

Rate of DMA bus is up to 1MHz,So each channel can work up to 64 kHz(read out Freq.) 16ch x 64kHz =1MHz

SA : START ADDRESS
EA : END ADDRESS
LA : LOOP POINT ADDRESS

65040G-099

E	$\overline{CS}$	A_3	A_2	A_1	A_ϕ	D7	D6	D5	D4	D3	D2	D1	D0
↓	0	0	0	0	0	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
		0	0	0	1	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
		0	0	1	0	—	—	—	Page R2 / PA2	Page R1 / PA1	Page R0 / PA0	SA17	SA16
		0	0	1	1	EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
		0	1	0	0	EA15	EA14	EA13	EA12	EA11	EA10	EA9	EA8
		0	1	0	1	Loop SW	Synch SW	—	—	—	—	EA17	EA16
		0	1	1	0	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
		0	1	1	1	LA15	LA14	LA13	LA12	LA11	LA10	LA9	LA8
		1	0	0	0	—	—	—	—	—	—	LA17	LA16

Loop SW
0 : Loop OFF
1 : Loop ON

Synch SW
0 : Synchro OFF
1 : Synchro ON

65030G-043

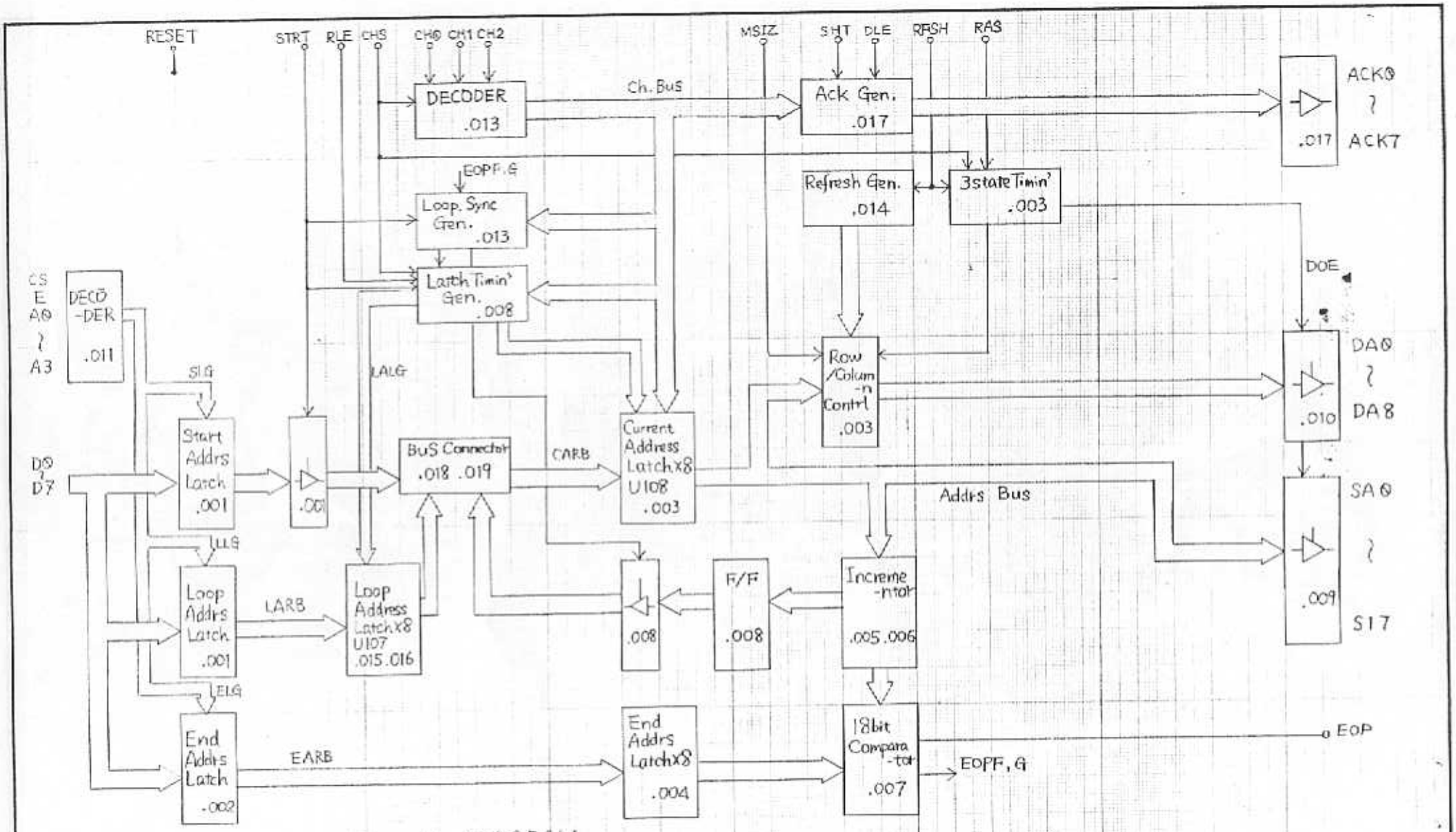
E	$\overline{CS}$	R/W	D7	D6	D5	D4	D3	D2	D1	D0
↓	0	0	—	WRITE (ch0)	ZeroX START SW	START ch MSB	START ch B4	START ch B3	START ch B2	START ch LSB
—	0	1	MPU WE	—	—	—	—	—	—	—

WRITE
0 : ch0 Read
1 : ch0 Write

START ch
: 00 ~ 23

ZeroX START SW
0 : ZeroX
1 : Forced

MPU WE
0 : DISABLE
1 : ENABLE

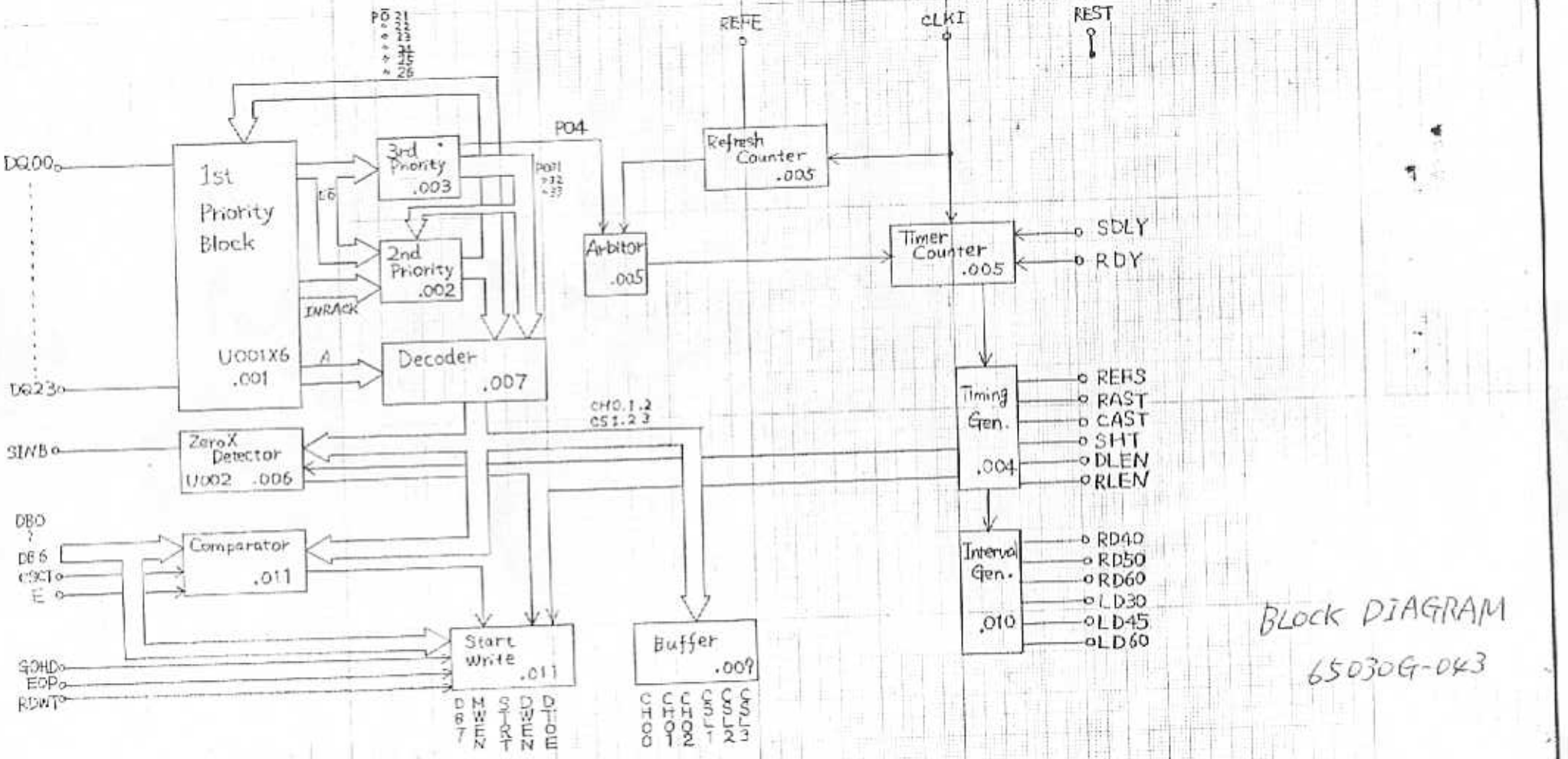


BLOCK DIAGRAM
65040G-099

PART NO.	NAME OF PART	MATERIAL	NO. OF PART	WEIGHT	REMARK
TREATMENT	DRAWN BY	DESIGNED BY	CHECKED BY	MODEL X-68000	DATE 60.5.27
				TITEL DMA GA-II Block Chart	REVISAL NO.
KORG KEIO ELECTRONIC LAB., CORP.			SCALE /	DRAWING NO. Y Sakurai	

REVISAL REASON	REVISAL DATE	REVISED BY

COMMERCIAL TOLERANCE ± %



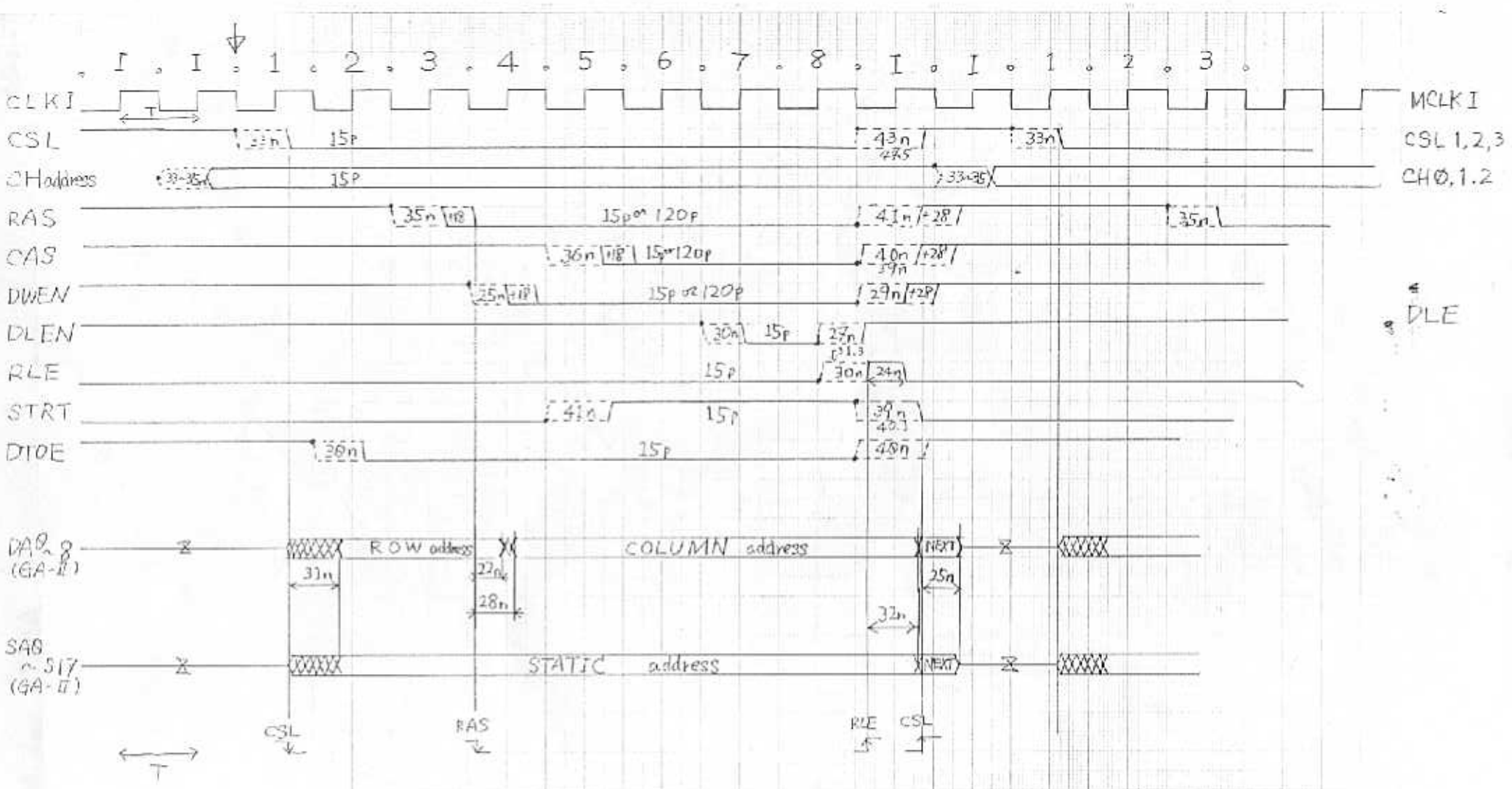
BLOCK DIAGRAM

65030G-0K3

PART NO.	NAME OF PART	MATERIAL	NO. OF PART	WEIGHT	REMARK
TREATMENT	DRAWN BY	DESIGNED BY	CHECKED BY	MODEL X-600	DATE 85.5.28
				TITEL GA-1 70-751	REVISAL NO.
KORG KEIO ELECTRONIC LAB., CORP.			SCALE /	DRAWING NO. Y.Sekiai	

REVISAL REASON	REVISAL DATE	REVISED BY

COMMERCIAL TOLERANCE ± %



$T = 1/f_{OSC} = 62.5\,nS\ (32MHz)$

85.5.17

TIMING DIAGRAM

65Ø3ØG-Ø43 → 65ØXØG-Ø99

C4/C5
60.3.22

Three Modes DMA

—normal. Loo: n:2—