Integrated Circuit Systems, Inc.

ICS 1261 (DOC1)

Digital Oscillator Chip

GENERAL DESCRIPTION

The ICS 1261 digital oscillator chip was designed by Ensoniq, the leading U.S. manufacturer of electronic keyboard musical instruments, to provide high quality electronic music synthesis capabilities for any music related applications. These applications range from professional music products (synthesizer's etc.) to arcade or home video games. The 1261 chip contains 32 digital oscillators, various control registers and an A/D converter.

Theory of Operation

There are 32 oscillators in the chip. Each oscillator is controlled by a set of seven registers:

1. Frequency Low
2. Frequency High
3. Volume
4. Data Sample
5. Address Pointer
6. Control Register
7. Resolution/Table Size Registers

In addition to these 224 oscillator control registers, there are three other registers:

1. Oscillator IRQ
2. Oscillator Enable
3. Analog to Digital Converter

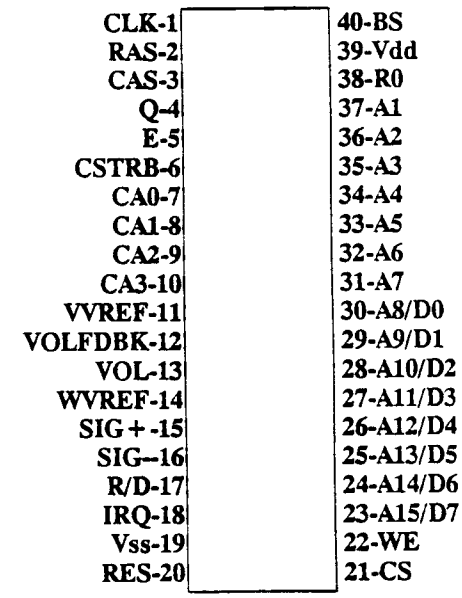
The seven oscillator control registers are grouped as 7 sets of 32 registers. In other words, all 32 frequency low control registers are grouped together and addresses consecutively, e.g., frequency low for oscillator 0 is address at location $00,OSC 1 frequency low is at $01. Frequency High Control for OSC is at $20, which is 32 locations above frequency low control. The register map for each of the seven oscillator control groups is as follows:

Address	Register Function Description
00-1F	Frequency low for OSC 0 thru OSC 31
20-3F	Frequency high for OSC 0 thru OSC 31
40-5F	Volume
60-7F	Waveform Data Sample
80-9F	Address Pointer
A0-BF	Control Register
C0-DF	Resolution/Table Size
E0	Oscillator Interrupt Register
E1	Oscillator Enable Register
E2	Analog to Digital Converter

FEATURES

- Directly addresses 64k bytes of memory
- Bank select output expands addressing to 128k bytes of memory
- Allows waveform output to be assigned to different channels (voices)
- Generates clock signals compatible with the Motorola 6809e microprocessor (E & Q clock inputs)
- Generates the row and column address strobes used by dynamic memories (RAS & CAS)
- Automatically refreshes 64k x 1 compatible dynamic memories
- On chip 8 bit linear Analog to Digital converter

Connection Diagram



Digital Oscillator Chip

CONTROL REGISTER (AO-BF)

The following chart indicates the decomposition of the control register into its bit definitions:

D7	D6	D5	D4	D3	D2	D1	D0
CA3	CA2	CA1	CA0	IE	M2	M1	H

For each OSC the control register is used to control three functions.

1. Channel Assignment (CA3-CA0)

Bits 7 thru 4 of the control register are defined as CA3 thru CA0. These four bits are used to control the final voice multiplexer. Sixteen different channel assignments are possible; only eight are normally used. Channel assignment is usually synonymous with voice assignment. Channel assign outputs can also be used for stereo pan.

2. Interrupt Assignment (IE)

Bit 3 of the control register is used to stop an interrupt from being passed to the Oscillator Interrupt Register (OIR). If IE is set, then the oscillator will cause an interrupt to be passed to the OIL when it completes a cycle, which in turn will interrupt the processor. If IE is clear, then the interrupt will be put into the oscillator ;interrupt table, but not passed to the OIR. When more than one oscillator interrupt occurs, the interrupt stack will retain the status and pass interrupts to the OIR as they are serviced by the processor. If the interrupt has been stored into the interrupt table while IE = 0, when IE is changed to a 1 the IRQ will be passed to the OIR.

Oscillator Mode (M2, M1,H)

Bits 2,1,0 control the functional mode of each oscillator.

The following chart describes these modes:

M2	M1	Oscillator Mode
0	0	Free Run
0	1	Address one cycle, reset OSC accumulator to zero, and set halt bit.
1	0	Sync OSC 2 to OSC 1 or amplitude modulated OSC 1 by OSC0 If set for an Even voice the the Odd voice will sync to the Even voice. It will reset the accumulators for both the Even and Odd voices to zero and the cycle will start again. If set for an Odd voice then the Odd voice envelopes the next Even voice. Note: voice 0 has no modulation source.
1	1	Address one cycle, reset OSC accumulators to zero, and set halt bit then reset halt bit of associated oscillator (toggle mode).

Whenever the halt bit is set by DOC or the processor and M1 is set, the OSC will be reset to zero.

M1 * H = 1 causes oscillator to be reset

Sync will cause OSC 2 to sync to OSC 1 in each voice group. (OSC 6 syncs to OSC 5 for voice 1 etc.)

Amplitude modulation will cause OSC 0 to be used as an envelope for OSC 1 in each voice group. (OSC 4 modulates OSC 5 in voice 3 etc.) Volume for OSC 0 and OSC 1 is ignored.

Digital Oscillator Chip

DATA SAMPLE (60-7F)

This set of registers is used to indicate the current 8-bit value of the waveform sample. This value will be fed to the D/A for that particular oscillator. This function is useful for LFO or modulation applications where the DOC oscillators are used to fetch sine wave samples that can be read by the processor for additional processing. These registers are read only.

VOLUME (40-5F)

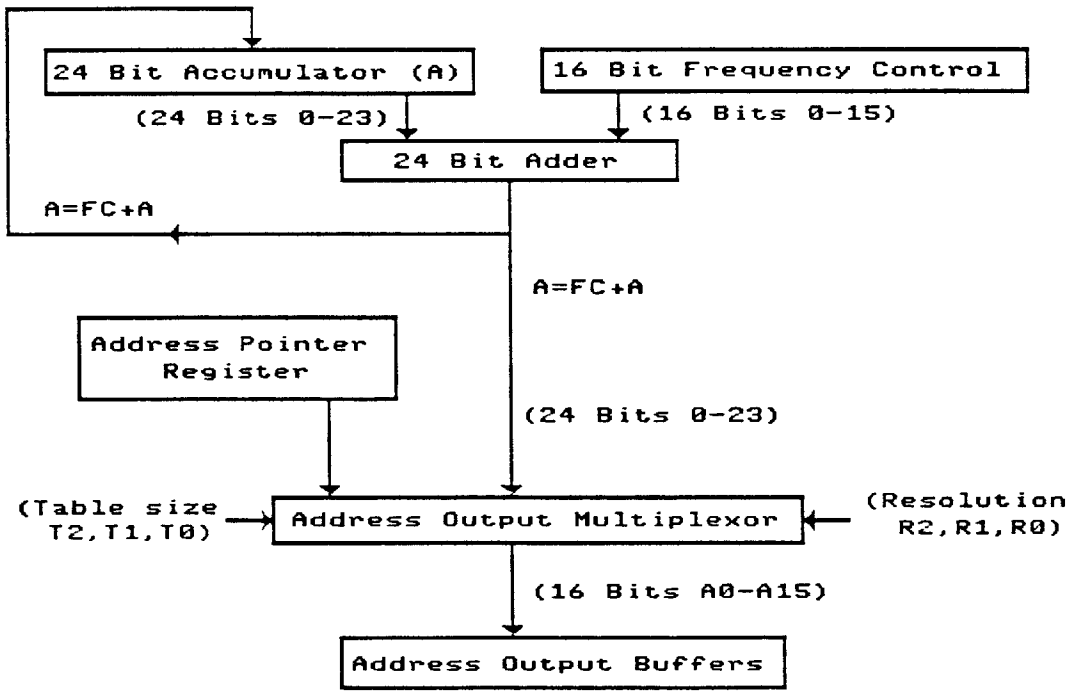
This set of registers is used to control the volume level of the waveform data. The 8-bit volume level is multiplied by the 8-bit waveform value to form the final analog output for each oscillator.

FREQUENCY CONTROL HIGH AND LOW (00-3F)

This group of registers is the 16 bit value which defines in part the actual frequency of the oscillator. These two registers are concatenated and become the incremental value for the linear accumulating oscillators. Determination of frequency out is as follows:

$$F_{out} = \frac{CLK}{8} \frac{FC}{(\#OSC + 2)\,(2^{(17+RES)})}$$

The oscillator block diagram is indicated below:



Digital Oscillator Chip

ADDRESS POINTER (80-9F)

This is an 8-bit register which defines the starting base address of the waveform table. The number of address pointer bits actually used in the final address depends on the size of the waveform table specified. The following chart indicates the use of the pointer bits:

WAVEFORM TABLE SIZE	A15	A14	A13	A12	A11	A10	A9	A8
256	P7	P6	P5	P4	P3	P2	P1	P0
512	P7	P6	P5	P4	P3	P2	P1	
1024	P7	P6	P5	P4	P3	P2		
2048	P7	P6	P5	P4	P3			
4096	P7	P6	P5	P4				
8192	P7	P6	P5					
16384	P7	P6						
32768	P7							

WAVEFORM TABLE SIZE/RESOLUTION/BANK SELECT (CO-DF)

This register controls three oscillator functions. The following chart indicates the bit position within the register to control three functions.

D7	D6	D5	D4	D3	D2	D1	D0
N.U.	BS	T2	T1	T0	R2	R1	R0

1. Bank Select Bit (B.S. = bit 6)

This bit is used to extend the addressing range of the DOC from 64K to 128K.

2. Table Size (T = b5, b4, b3)

These 3-bits are used to specify the size of the waveform table addressed by the oscillator.

T2	T1	T0	Table Size
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

3. Resolution

These three bits determine which set of 16 bits, of the 24 in the oscillator accumulator, are used to address the waveform table. The purpose of this accumulator bit selection is to allow the frequency resolution to be adjusted to the waveform table size. For example, when using a 32K waveform table, accumulator bits 8 thru 23 would normally be used, but in a 256 byte table a lower resolution setting would be used to step through the table faster.

There are eight accumulator address bit selections available.

R2	R1	R0	Accumulator Bits Used as Addresses
0	0	0	16 through 9-T
0	0	1	17 through 10-T
0	1	0	18 through 11-T
0	1	1	19 through 12-T
1	0	0	20 through 13-T
1	0	1	21 through 14-T
1	1	0	22 through 15-T
1	1	1	23 through 16-T

Digital Oscillator Chip

OSCILLATOR INTERRUPT REGISTER

The OIR is used to inform the processor which oscillator has caused an interrupt request occur. When an oscillator completes a waveform table an interrupt is generated. This interrupt will be passed to the OIR if IE = 1. The OIR will then issue an IRQ to the processor. Upon recognizing the IRQ, the processor reads the OIR to determine which oscillator issued the IRQ. The OIR is an 8-bit register where Bit 7 indicates the state of the IRQ line. (bit 7 = 0 for valid IRQ. Bits 5 through 1 contain the oscillator number 0 through 31. Bits 6 and 0 are always 1.

D7	D6	D5	D4	D3	D2	D1	D0
IR	1	04	03	02	01	00	1

After the processor reads the OIR, the DOC will clear the appropriate oscillator interrupt request, e.g., if oscillator 4 causes an IRQ, then the processor will read: OIR = 65 + 4.

OSCILLATOR ENABLE REGISTER (E1)

This register determines the number of active oscillators on the DOC. Load the register with the number of oscillators to be enabled, multiplied by 2, e.g., to enable all oscillators, load register with a 62.

Note: There are 32 oscillators on DOC plus 2 additional time slot for RAM refresh. Therefore, 34 actual oscillator time slots are used. If the number of oscillators is halved to 16 the frequency is not doubled since the two refresh time slots still exist. To halve the frequency, the number of enabled oscillators should be 15. Oscillators which are disabled will not hold their associated register data since they are not refreshed.

ICS1261 Pin Descriptions

Pin Number	Signal Description	
1	CLK	**CLOCK INPUT** - Master clock for the 5503 chip. Must be 50% duty cycle. It is internally divided by 8 to get the basic cycle time.
2	$\overline{\text{RAS}}$	**ROW ADDRESS STROBE OUTPUT** - Strobe for accessing dynamic memory.
3	$\overline{\text{CAS}}$	**COLUMN ADDRESS STROBE OUTPUT** - Strobe for accessing dynamic memory.
4	Q	**Q CLOCK OUTPUT** - Compatible with the M6809E microprocessor Q clock. This clock leads the E clock (pin 5) by 1/4 cycle and has a 50% duty cycle.
5	E	**E CLOCK OUTPUT** - Compatible with the M6809E microprocessor E clock. This clock also has a 50% duty cycle
6	$\overline{\text{CSTRB}}$	**CHANNEL STROBE OUTPUT** - Low active signal indicates when the channel assign outputs (CA0 - CA3) are valid.
7-10	CA0-CA3	**CHANNEL ASSIGN OUTPUTS** - Allows the outputs of the oscillators (SIG+ & SIG-) to be directed to different channels.
11	VVREF	**VOLUME VOLTAGE REFERENCE INPUT** - Reference voltage for the internal volume D/R converter. Must be -5v + or - 5%.
12	VOLFDBK	**VOLUME FEEDBACK INPUT** - This pin is tied to an on-chip resistor to pin 13 that can be used as the feedback resistor with an external op-amp to generate the waveform D/A voltage reference.

Digital Oscillator Chip

ICS1261 Pin Descriptions (contd)

13	VOL-	VOLUME OUTPUT - This signal is a current output which should be converted to a voltage, the output of which is fed into the WVREF input (pin 14). This voltage will be used as the reference voltage for the internal D/A converter for the SIG+ and SIG- outputs. It must also be fed back into the volfdbk input (pin 12).
14	WVREF	WAVEFORM VOLTAGE REFERENCE INPUT - This input will provide the reference voltage for the internal D/A converter for the SIG + and SIG- output (pins 15 & 126).
15-16	SIG+ SIG-	WAVEFORM SIGNAL + AND - OUTPUTS - These two outputs are differential currents representing the final waveform output value (sample).
17	A/D	ANALOG/DIGITAL CONVERTER INPUT - This is the input for the analog to digital converter on the ICS1261 chip. The conversion time is 30 usec and the input range is 0v to 2.5v. The linearity error is + or - 1/2 LSB.
18	$\overline{IRQ}$	INTERRUPT REQUEST OUTPUT - This low active signal indicates that one or more oscillators have completed their cycle. This output can be disabled through the individual oscillators control registers. It is an open collector output.
19	V_{ss}	VOLTAGE INPUT - This is the ground reference for the ICS1261 chip.
20	RES	RESET INPUT - This pin when low will internally reset the ICS1261's registers.
21	$\overline{CS}$	CHIP SELECT INPUT - This pin when low will enable the ICS1261 to communicate with a microprocessor or other controlling device.
22	$\overline{WE}$	WRITE ENABLE INPUT - This pin is the read/write signal for the ICS1261. A high signal on this pin initiates a read cycle and a low signal on this pin initiates a write cycle.
23-30	A15/D7 A8/D0	ADDRESS/DATA LINES INPUT/OUTPUT - These pins are address lines A8-A15 and data lines D0 - D7 when the ICS1261 is accessing waveform data (E clock output is low) and they are data lines D0-D7 when the ICS1261 is being accessed by an external controlling device (E clock output is high).
31-38	A0-A7	ADDRESS LINES INPUT/ OUTPUT - These pins are address line A0-A7 or when the ICS1261 is accessing waveform data and are address lines A0-A7 in when the ICS1261 is being accessed by an external controlling device.
39	V_{dd}	VOLTAGE INPUT - This is the positive power supply pin - +5v + or - 5%.
40	BS	BANK SELECT OUTPUT - This output pin is essentially address line A16.

Digital Oscillator Chip

ICS1261 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	-10 to 80 degrees C
Storage Temperature	-65 to 150 degrees C
Voltage on any Pin	-0.3V to +7V

D.C. CHARACTERISTICS

T_a = 0 to 50 degrees C, V_{dd} = 5v +/-5%

CHARACTERISTICS	MIN.	MAX.	TYP.	UNITS
R/W,CS,A0-A7, A8/D0-A15/D7,RES				
V_{il}	0.0	0.4	-	Volts
V_{ih}	2.4	5.0	-	Volts
CSTRB,CA0-CA3, VSTRB,WSTRB,BS, A0-A7, A8/D0 - A15/D7				
V_{ol}	-	0.8	-	Volts
V_{oh}	2.4	-	-	Volts
I_{ol} - Sink Current, Vol=0.4	-	2.0	-	mA
I_{oh} - Source Current, Voh = 2.4	-	1100	-	µA
CLOCK INPUT (CLK)				
Frequency	-	10	8	Mhz
V_{il}	0.0	0.4	-	Volts
V_{ih}	4.5	-	-	Volts
CLOCK OUTPUTS (RAS, CAS ,E ,Q)				
Frequency (RAS, CAS)	-	-	2	Mhz
Frequency (E,Q)	-	-	1	Mhz
V_{ol}	-	0.8	-	Volts
V_{oh}	2.4	-	-	Volts
I_{ol} - Sink Current, Vol = 0.4	-	2.0	-	mA
I_{oh} - Source Current, Voh = 2.4	-	100	-	µA

ICS1261 SYSTEM TIMING

INPUT CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Clock Cycle Time	T_{cyc1}	100	125	200	ns
Clock High	T_{pwh}	50	-	-	ns
Clock Low	T_{pwl}	50	-	-	ns
Rise and Fall Times	T_r, T_f	-	-	10	ns

OUTPUT CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Two MHz Clock Cycle Time	T_{cyc2}	480	-	500	ns
RAS/CAS Clock Output High	T_{oh1}	270	-	290	ns
RAS/CAS Clock Output Low	T_{ol1}	190	-	210	ns
RAS High after E Low	T_{rd}	-	-	40	ns
CAS High after RAS High	T_{cd}	40	-	70	ns
1MHz μProcessor Clocks Cycle Time	T_{cyc3}	980	-	1000	ns
E/Q Clock Output High	T_{oh2}	480	-	500	ns
E/Q Clock Output Low	T_{ol2}	480	-	500	ns
E High from Q High (*Q leads E*)	T_{qd}	240	-	250	ns
Rise and Fall Times (E,Q,RAS,CAS)	T_r,T_f	-	-	10	ns

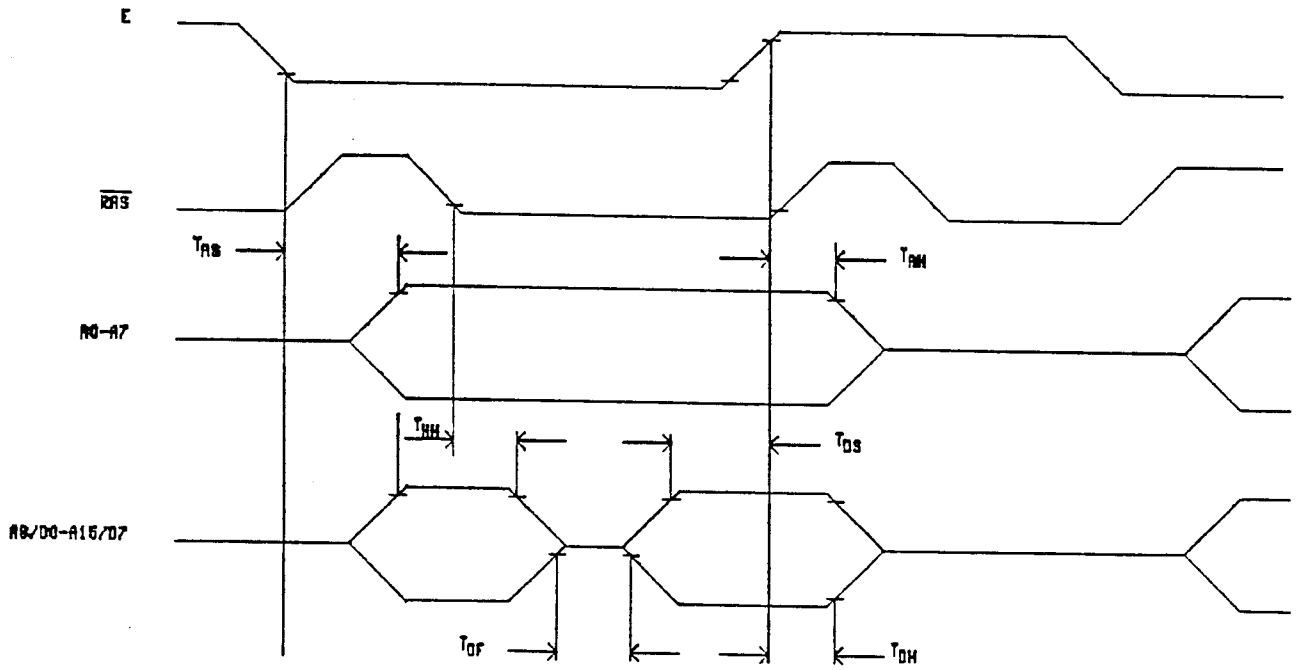
MICROPROCESSOR READ/WRITE TIMING TO ICS1261

CHARACTERISIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Address Setup Time	T_{as}	350	-	-	ns
Address Hold Time	T_{as}	0	-	100	ns
R/W Signal Delay from E Low	T_{rs}	-	-	100	ns
R/W Signal Valid for Read	T_{rw}	350	-	-	ns
Chip Select Hold From E Low	T_h	0	-	-	ns
Data in Setup Time	T_{ds}	150	-	-	ns
Data in Hold Time	T_{dh}	30	-	-	ns
R/W Signal Valid for Write	T_{ww}	350	-	-	ns
Data Out Hold Time	T_{dh}	30	-	-	ns

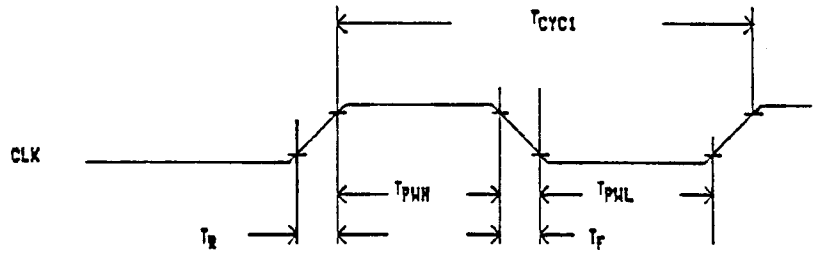
ICS1261 System Timing (contd.)

ICS1261 READ FROM MEMORY

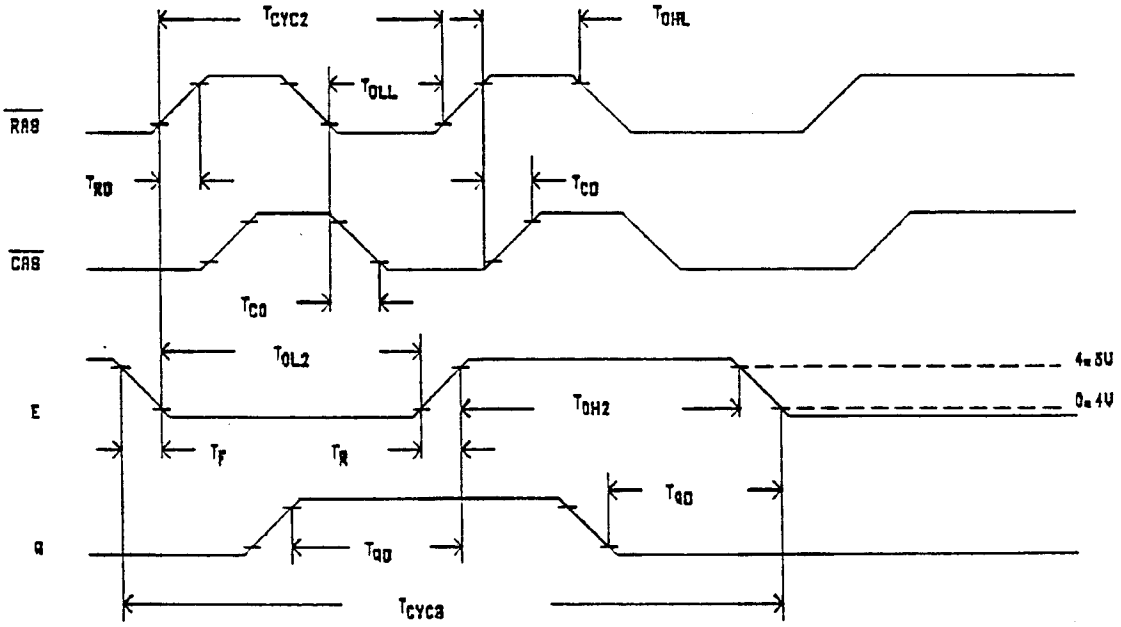
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Time to Valid Address From E	T_{as}	-	-	50	ns
Address Hold Time (A0-A7)	T_{ah}	0	-	10	ns
A8 - A15 Hold Time From RAS Fall	T_{hh}	-	-	30	ns
A8/D0 - A15/D7 Lines Switching Time	T_{of}	30	-	-	ns
Data in Setup Time	T_{ds}	100	-	-	ns
Data in Hold Time	T_{dh}	20	-	-	ns



ICS 1261 Read From Memory



ICS1261 Input Clock



ICS1261 Output Clocks

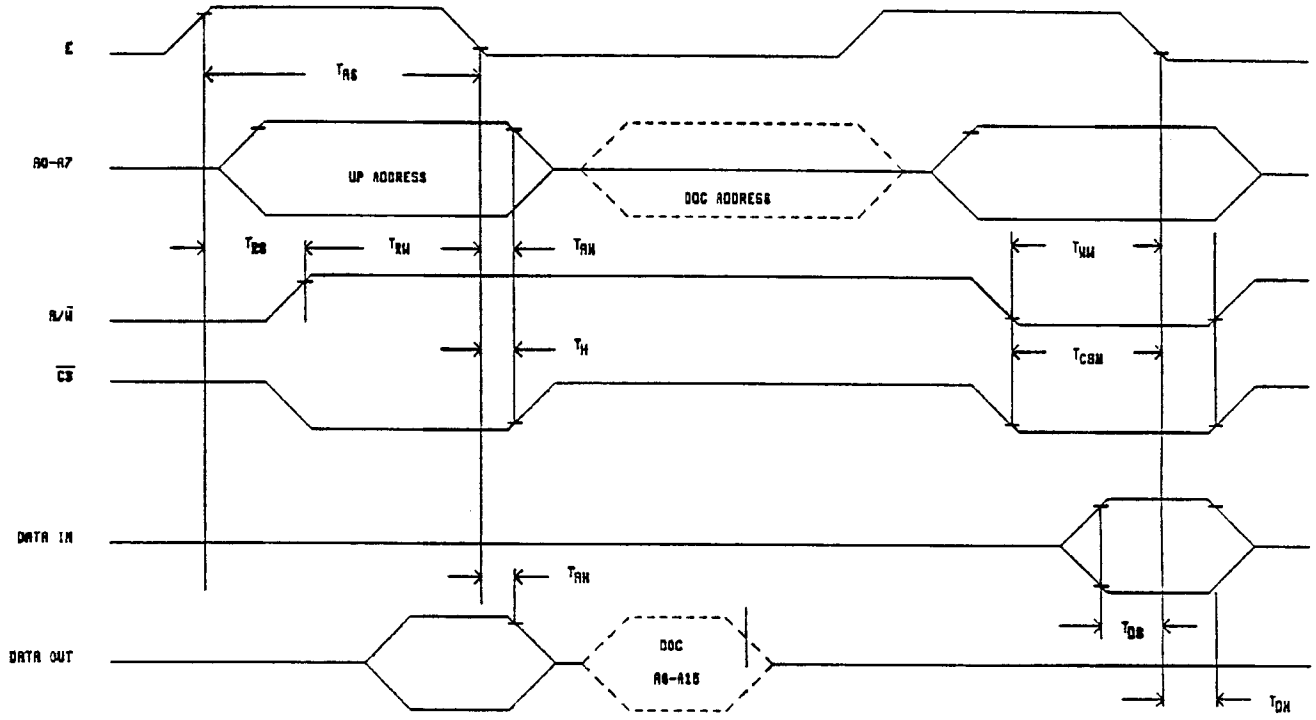
Digital Oscillator Chip

Final Address Calculation

The final address can be calculated using the following table.

TABLE SIZE	FINAL ADDRESS																RESOLUTION		
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R2	R1	R0
256	P7 ← POINTER REGISTER → P0								A23 ← ACCUMULATOR BITS → A16							A16 A9	1 ↓ 0	1 ↓ 0	1 ↓ 0
512	P7						P1	A23 A16								A15 A8	1 ↓ 0	1 ↓ 0	1 ↓ 0
1024	P7					P2	A23 A16									A14 A7	1 0	1 0	1 0
2048	P7				P3	A23 A16										A13 A6	1 0	1 0	1 0
4096	P7			P4	A23 A16											A12 A5	1 0	1 0	1 0
8192	P7		P5	A23 A16												A11 A4	1 0	1 0	1 0
16384	P7	P6	A23 A16													A10 A3	1	1	1
32768	P7	A23 A16														A9 A2	1 0	1 0	1 0

For example, a waveform that is 512 bytes long, and the resolution register is set for 7, then pointer bits 1 through 7 and accumulator bits 15 through 23 will make up the final address. If the resolution register were now changed to 5,then pointer bits 1 through 7 and accumulator bits 12 through 21 would make up the final address.



Microprocessor Read / Write Timing to ICS1261

Integrated Circuit Systems, Inc.

Valley Forge Corporate Center

2626 Van Buren Ave., P.O. Box 968

Valley Forge PA 19482-0968

(215)666-1900

FAX (215)666-1099